supplying customized ICs

aptasic

Technical Documentation

Generic Qualification Flow for Plastic Packages

Aptasic_Plastic-Qualification_en_20110728-AQ-draft
2011.07.28 10:20

Generic Qualification flow for Plastic Packages

aptasic

01: Solderability	02: ESD	03: TempCycling	04: Humidity	05: LifeTest
Parts numbering 15 ICs	**Parts numbering** 3 x 3 ICs	**Parts numbering** 77 ICs	**Parts numbering** 77 ICs	**Parts numbering** 77 ICs
	Begin test room / +85°C	**Begin test** room / +85°C	**Begin test** room / +85°C	**Begin test** room/-40°C/+85°C
		Temp-cycling *JESD22-A104* -40°C/ +125°C 100 cycles NO bias applied	**HTSL** *JESD22-A103* +125°C / 24 h NO bias applied	**HTOL** *JESD22-A108* 125°C / 160h Vdd max Biased
	Diode curves before ESD test	**Interim test 1** room temp	**Interim test 1** room temp	**Interim test 1** room temp
Solderability test *J-STD-002C* test E ROL1 flux SAC305 alloy	**ESD test** *JESD22-A114* Verification test room temp 1/2/4 kV HBM	**Autoclave** *JESD22-A102* 121°C/100%RH 205kPa/96h NO bias applied	**Temp-cycling** *JESD22-A104* -40°C/ +125°C 10 cycles NO bias applied	**HTOL** *JESD22-A108* 125°C / 840h Vdd max Biased
	Diode curves after ESD test		**Interim test 2** room temp	
	Validation Comparison of the curves after vs. before		**THB** *JESD22-A101* +85°C / 85 %RH 500 h Vdd max Biased	
			Interim test 3 room temp	
			THB *JESD22-A101* +85°C / 85 %RH 500 h Vdd max Biased	
	Final test room / +85°C	**Final test** room / +85°C	**Final test** room / +85°C	**Final test** room/-40°C/+85°C

Result evaluation
(FIT, Drift, Histograms)

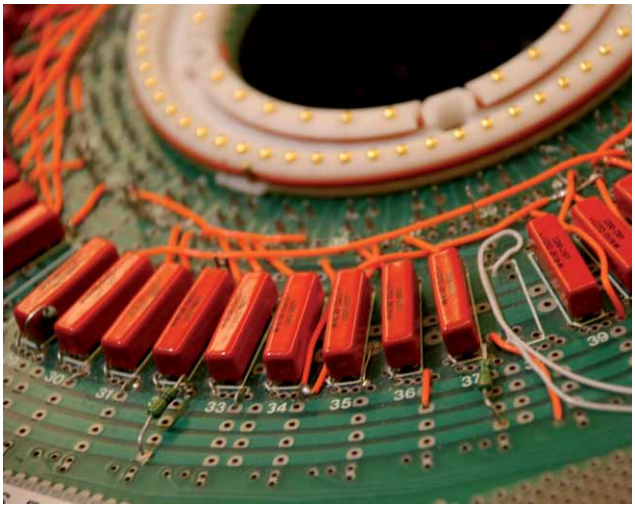
Qual report

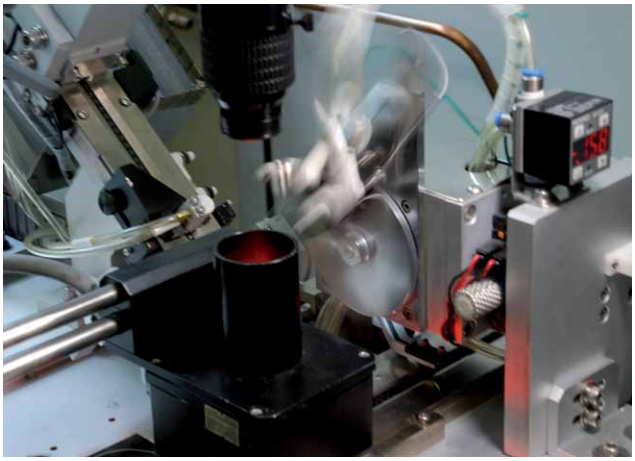
Additional Information

The proposed generic qualification flow applies for plastic packages. It is based on JEDEC and AEC-Q100 quality standards.

The latest release of the applicable standards can be downloaded from the JEDEC and AECcouncil download center:

- http://www.jedec.org/standards-documents
  Particular focus has been given on standard JESD47G.01 (Stress-Test-Driven Qualification of Integrated Circuits) and JESD22 series (Reliability Test Methods for Packaged Devices).
- http://www.aecouncil.com/AECDocuments.html





Abbreviation used

- **AC** AutoClave
- **ESD** Electro-Static Discharge
- **HAST** Highly-Accelerated temperature and humidity Stress Test
- **HBM** Human Body Model
- **HMM** Human Machine Model
- **HTOL** High Temperature Operating Life (=Life Test)
- **HTSL** High Temperature Storage Life
- **THB** Temperature Humidity Bias

Qualification parameters

Some of the parameters mentioned on the Generic Qualification Flow are given as examples.
Some of them might be subject to change, depending on the specification of the devices.
Concerned parameters are mainly:

- Temperatures (e.g. electrical test, temperature cycles)
- Supply voltages for biased stresses
- ESD test voltage levels
- Number of devices
- Solderability
- EEPROM retention

JESD47 - Stress-Test-Driven Qualification of Integrated Circuits

Scope: This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.
These tests are capable of stimulating and precipitating semiconductor device and packaging failures.
The objective is to precipitate failures in an accelerated manner compared to use conditions.

JEP122 - Failure Mechanism and Models for Silicon Semiconductor Devices

Scope: This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions.

JESD22 - Reliability Test Methods for Packaged Devices

- **A101** - **Steady State Temperature Humidity Bias Life Test**
  Scope: This test is performed to evaluate the reliability of non-hermetic packaged IC devices in humid environments. Temperature, humidity, and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulate or seal) or along the interface between the external protective material and the metallic conductors which pass through it.
- **A102** - **Accelerated Moisture Resistance - Unbiased Autoclave**
  Purpose & Scope: The « Unbiased Autoclave Test » is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive…
  This test is used to evaluate new packages or packages that have undergone changes in materials (e.g. mold compound, die passivation) or design (e.g. die/paddle sizes). However, this test should not be applied on laminate or tape based packages i.e. FR4 material, polyimide tape or equivalent.
- **A103** - **High Temperature Storage Life**
  Scope: The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices.
  High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any).
- **A104** - **Temperature Cycling**
  Scope: This test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes.
  Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses.
- **A108** - **Temperature, Bias, and Operating Life**
  Scope: This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way, and is primarily for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as burn-in, may be used to screen for infant mortality related failures.
- **A110** - **Highly-Accelerated Temperature and Humidity Stress Test**
  The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

Company at glance

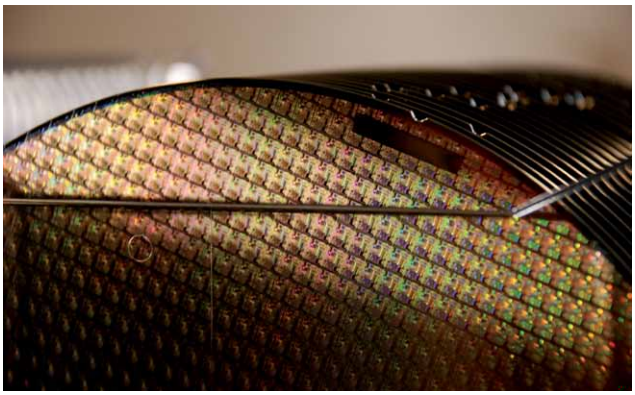
About Aptasic

Founded in 1979 under the name of CSEE with the main activity of testing electronic components and then Application Specific Integrated Circuits (ASICs), the company was acquired by the PQH group in 2006 and changed its name into Aptasic SA.

Activities and Services

Aptasic offers the whole supply chain related to the production of Integrated Circuits (ICs) and its field of expertise expanded to cover all aspects related to the manufacturing of good devices, namely:

- consulting in Design for Test, Design for Manufacturing, Design for Assembly (DfX) domains
- multi-site wafer probing at cold/room/hot temperature
- prototyping of small series (using ProtoPack)
- encapsulation in plastic and ceramic packages
- package test at cold/room/hot temperature
- screening and qualification procedures (according to JEDEC and MIL-883 standards)
- tape and reel (T&R)
- and many other specialized processing steps that can be applied on semiconductor industry



Vision

Enable our customers first time right production ramp-up, supporting smooth supply chain integration (from design to good packaged devices ready for use).

Mission

Offer to our customers, as main contractor, easy access to state-of-the-art foundries, assembly houses, production processes, technologies and consulting in the semiconductor industry.

Aptasic · Rte de la Gare 55a · CH-2017 Boudry · +41 0 32 729 11 30 · +41 0 32 729 11 39 · www.aptasic.ch ·